Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 7 (Cancelled).
- 8. (Currently Amended) A method of initialization for a multitone system, comprising:
 - (a) comparing upstream and downstream data rates for a two-band duplex to threshold data rates; and
 - (b) when said data rates fail to meet said threshold data rates in step (a),

 comparing data rates for a hybrid duplex to said threshold data rates, wherein said

 hybrid duplex uses hyperframes with structure:
 - (i) for each n where n is an integer with 1.ltoreq.n.ltoreq.N and N is an integer greater than

 2, a first sequence of n first frames set of symbols, referred to as a type 1

 symbols, for transmission in a first direction in a first set of subchannels and transmission in a second direction in a second set of subchannels where said first and second directions differ and said first and second sets are different; and
 - (ii) a second sequence of at least N-2-n second frames for transmission in said second

 direction in both said first set and said second set of subchannelsset of symbols,

 referred to as a type 2 symbols, where transmission is only in the first direction in

 the first set of subchannels; and
 - a third set of symbols, referred to as a type 3 symbols, where transmission is only in the

 first direction in subchannels different from that of the set of subchannels used for
 type 2 symbols.
- 9. (New) An article of manufacture in the form of a hyperframe for use in a communication system including a plurality of processor circuitry operable to provide a discrete multitone system, said article of manufacture comprising:

- a first set of symbols, manufactured by the plurality of processor circuitry from the data bits input, the first set of symbols referred to as a type 1 symbols, where transmission is in a first direction using a first direction set of subchannels and second direction using a second direction set of subchannels;
- a second set of symbols, manufactured by the plurality of processor circuitry from the data bits input, the second set of symbols referred to as a type 2 symbols, where transmission is only in the first direction using the first direction set of subchannels; and
- a third set of symbols, manufactured by the plurality of processor circuitry from the data bits input, the third set of symbols referred to as a type 3 symbols, where transmission is only in the first direction using subchannels different from that of the set of subchannels used for type 2 symbols,
- wherein the total of symbols is N symbols comprised of n1 type 1 symbols, n2 type 2 symbols and n3 type 3 symbols, where n1 + n2 + n3 = N.
- 10. (New) The article of manufacture of claim 9, wherein the set of subchannels used by the type 2 symbols for transmission in the first direction does not include the set of subchannels used for transmission in the second direction by the type 1 symbols
- 11. (New) The article of manufacture of claim 9, wherein the set of subchannels used by the type 3 symbols for transmission in the first direction includes the set of subchannels used for transmission in the second direction by the type 1 symbols.
- 12. (New) The article of manufacture of claim 9, wherein the N symbols are ordered such that there are n1 type 1 symbols, followed by 1 type 2 symbol, followed by n3 type 3 symbols, followed by 1 type 2 symbol.
- 13. (New) The article of manufacture of claim 9, wherein first direction is downstream and second direction is upstream.
- 14. (New). A method of initializing a discrete multitone system with a hyperframe in a communication circuitry including a signal processor, comprising:
 - determining the allowed set of PSD masks for first and second directions of type 1, type 2 and type 3 symbols;

determining a target data rate for the first and second directions;

including type 1 and type 3 symbols in the SNR measurement phase;

performing a bit loading for the type 1, type 2 and type 3 symbols to determine the data rates supported in the first and second directions for each type of symbol; and

signal processor manufacturing the hyperframe, said manufacturing comprising:

choosing all type 1 symbols if the type 1 symbol is able to meet the target data rates for the first and second directions; and

choosing a mix of type 1, type 2 and type 3 symbols to most closely meet the target data rates for the first and second directions if all type 1 symbols are unable to meet the target data rate.